Vikash Kumar

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Profile Summary

PDK Engineer with 5+ years of experience enabling signoff-quality physical verification decks across technology nodes from 180nm to 18nm. Expertise in LVS/PEX development, debug, and automation using Calibre nmLVS/nmDRC and Synopsys StarRC. Proven ability to improve verification efficiency, reduce turnaround time, and enhance PDK robustness through scalable automation and cross-functional collaboration. Strong track record supporting tapeout readiness in complex design environments.

Technical Skills

- **Physical Verification:** Calibre nmLVS/nmDRC (SVRF/TVF), Cadence PVS/Virtuoso, Rule Deck Development
- **Parasitic Extraction:** Synopsys StarRC, Cadence Quantus, Extraction Accuracy & Debug
- **Programming:** Python, Tcl, Shell (QA Automation, Flow Optimization)
- **Tools & OS:** Git, Linux, Windows

Professional Experience

PDK Engineer *STMicroelectronics, Greater Noida* [April 2023- Present]

- Developed and maintained LVS/PEX decks for 180nm–18nm nodes, enabling signoff-quality verification and supporting multiple successful tapeouts.
- Drove LVS/PEX debug for internal design teams and external customers, resolving complex mismatches and extraction issues to accelerate verification closure.
- Supported verification readiness for design cycles, contributing to tapeout-level robustness and consistency of PDK deliverables.
- Built scalable Python/Tcl-based QA automation frameworks, reducing manual validation effort by 30% and improving turnaround time for deck release cycles.
- Collaborated with cross-functional CAD and design teams to enhance PDK usability, coverage, and reliability across multiple projects
- Trained and mentored 3 engineers and 1 intern on PDK workflows, tools, and verification methodologies.

PDK Engineer *Sevya Multimedia (On-site at STMicroelectronics)* [April 2021- March 2023]

- Developed and validated LVS/PEX decks for multiple process nodes, strengthening physical verification flows and improving deck stability.
- Automated QA validation checks using Python, improving coverage and reducing manual verification overhead.
- Debugged LVS mismatches and parasitic extraction issues in collaboration with design teams, improving turnaround time for issue resolution.
- Designed QA validation structures to ensure correctness, completeness, and consistency of rule decks.
- Contributed to production-grade PDK workflows through SVRF rule writing, device recognition, and connectivity extraction.

Trainings

SKILL Coding: Layout Automation *STMicroelectronics* [May 2024]

- Developed automation scripts for Virtuoso database operations, improving layout productivity and reducing manual effort.

Calibre: Writing DRC/LVS Rules *Siemens EDA* [July 2023]

- Hands-on experience in SVRF/TVF rule development, device recognition, connectivity extraction, and advanced LVS debugging.

Education

2017-21 B.Tech Hons.(ECE) Silicon Institute of Technology, Bhubaneswar 8.7/10